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PAPER

Fractional analog scheme for efficient stabilization of a synchronous buck converter

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This paper presents the design and control of power electronic synchronous buck converter. Even though a synchronous buck converter is more popular and more widely available, it is not always efficient as nonsynchronous. Firstly, the input-output linearization from the state space averaging of the converter is studied, after which a small AC signal analysis is introduced to obtain the dynamic transfer function. All the parameters of the converter are calculated based on the output voltage, current ripples as well as the input voltage. For robustness, the controller is implemented by comparing the response of integer order with non-integer (fractional) order controller, simply known as fractional order controller (FOC). The fractional order derivative is implemented from the Oustaloup approximation and the controller parameters are being tuned using Nelder Mead approximation bases on a system model. It is shown that the FOC performance is comparatively better in presence of the load disturbances and parameter variations. The experimental study with the real-time fractional PI is possible to make for a stand-alone embedded application using FPAA. The proposed technique does not require any digitization of the signal, so it can be easy to implement with improved performance. The effectiveness of the analog controller is discussed, giving some future directions to adopt the new fractional controller.

K e y w o r d s: DC-DC buck converter, Fractional Controller, FOPI, FPAA

1 Introduction

Most of the electronic devices nowadays depend on the DC current and are becoming more valuable and expensive due to its strong performance. In addition, most of the devices acquire certain amount of voltage or are designed to operate only in a specific manner or in a certain range of voltage. Therefore, power conversion was introduced in the past decades as the solution to the rising issue.

Apart from the introduction of a DC buck converter, the controller is designed to interface with the power conversion to produce stabilized output [1]. The purpose of the controller is to compare the output voltage with reference voltage and ensure that output voltage must be equivalent to the reference voltage. The buck converter is used to step down the voltage from the source into the required regulated voltage. The role of the controller is to then compare the voltage to determine if the reference voltage still greater. A key task is to ensure that the incoming input voltage must be step down to the voltage required.

PID controller was proven as a reliable tool which was used in industries due to the performance as the machines have stable function in experimentation. Furthermore, it is used regularly, available commercially and easy to implement for various dynamic functions to eliminate steady state response. However, there are a number of controllers have been designed recently and are unique due to their performance attribute. The couple inductor technique for high step DC/DC converter with MPPT control was proposed by Sundar *et al* [2]. The IMC was proposed as a robust output regulator for a DC/DC buck converter in [3]. This scheme does not require the precise system parameters and is simple to implement.

Since the robust output regulation problem of the converter can be converted into a robust stabilization problem of an augmented system consisting of the given buck converter, can be overcome by introducing a proper internal model. Therefore, the proposed controller successfully solved the DC/DC buck converter based on internal mode with a conditional integrator and robust sliding stabilizer [4]. In the last few years, the fractional-order controller, commonly known as FOPID, was developed for more precise tuning and robust performance [5 and references within]. The introduction of the fractional controller is one-step closer to the real world situation because most of the issues are rational problems [6, 7].

It is always a subject of research to overcome the damaging influence of load and voltage deviations in regulators. A step down buck converter is widely used with high output power due to its high efficiency and small size. To get high efficiency from the output voltage, the DC/DC buck converter must be constructed using an ideal impedance, where the required impedance must dissipate less amount of energy. The non-ideal nature of the switches and other impedance in conduction mode uses power in different form and as a result, current and volt-

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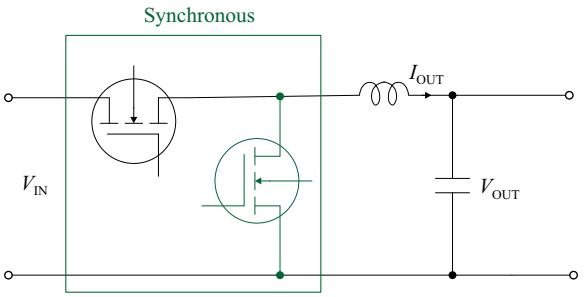

Fig. 1. Synchronous buck converter topology

age cannot be zero in switching mode and so, it is found that its efficiency is around 70 % to 90 % [8, 9]. Nevertheless, the buck converter performance is highly sensitive to parameter variations, large supply, load variations and nonlinearity. This motivated the authors to investigate a new control strategy, which focuses on the analog controller with fractional behavior.

Recently, Soman *et al* [10] presented a technique to determine DC-DC buck converter transient dynamics and designed the analog controller using the soft-start capacitor. A sliding mode control based robust method was presented in [4] for the same problem. It is shown that such nonlinear control can make the system less sensitive to disturbance and parameter variations. However, such method is very costly to implement in real time environment.

Apart from many controller strategies that have been used to improve DC-DC buck converter, a fractional order controller and its actual implementation is yet to be verified in detail. A fractional sliding mode control scheme was first proposed in [11] to control such devices. The sliding surface was designed through PID/PI structure and controller algorithm was implemented in a computer machine.

This paper presents an analog controller design to monitor the output voltage of synchronous DC buck converter. The system is modelled first in simulation environment before implementation on the hardware. In order to setup synchronous buck, a dead time circuit is designed to create a delay time between the switching of two MOSFETs. As for any driver circuit or controller, it is to ensure that both MOSFETs are not activated simultaneously. The practical results depict that the synchronous buck converter is more efficient compared to the conventional controller and resulted in being 5% more efficient in the presence of load disturbances and parameter variations. Importantly, it is shown in experimental study that the real time fractional PI controller is possible to make for a stand-alone embedded application using FPAA. This analog controller does not require any digitization of the signal, therefore, it is much easier to implement with improved performances. In addition, the PWM can be realized together with FOPI without additional circuit components. Finally, a synchronous converter is implemented fully with the FPAA in a loop to correlate the theoretical assumption and real-time measurement.

2 Background theory on synchronous buck converter

Figure 1 shows a general configuration of a synchronous buck converter. In this configuration, an active switch is used, such as power MOSFET, and the diode rectifier is replaced as in a conventional buck converter.

Due to on-voltage drop being less than the forward voltage drop of the rectifier, the efficiency increases. In other words, it is desirable to reduce the on state voltage drop for the rectifier where one can minimize the conduction loss when the current is flowing through this path. In addition, this topology is used to prevent cross conduction and reverse recovery of the parasitic PN diode internal to a MOSFET [9]. The driver circuit or controller used in this converter must ensure that both MOSFET are not active simultaneously. Another characteristic of the synchronous buck converter is that it always operates in Continuous Conduction Mode (CCM) since current is reverse in replaced switch. Thus, the regulated voltage relationship and the duty-cycle-to-output voltage transfer function are the same as in conventional buck DC-DC converter.

The parameters of this converter, such as inductor and capacitor, are determined as per the design. Assuming that the input applied voltage is V_{in} and nominal output voltage is V_{out}, from Fig. 1, it can be seen that it is nothing but a LC filter circuit which receives a voltage square wave as its input given by the control switching action of the two MOSFET. After a proper filtering, a regulated output voltage V_{out} is obtained. However, for the complete power supply, which is made up of power stage and a control circuit, it usually must meet a set of minimum performance requirement, referred to as the power supply specification.

In [8], the control strategy with duty cycle PWM is presented for the buck converter. It is noted that the duty cycle can vary in order to control the output voltage, hence the transfer function is obtained as

$$\frac{V_c(s)}{D(s)} = \frac{u_1}{1 + s\frac{L}{R} + s^2 LC}\,. \tag{1}$$

This transfer function is a damped second order low pass filter response where u_1 is the DC gain. The natural frequency and the damping ratio are given by

$$\textit{Natural Frequency} = \frac{1}{2\pi\sqrt{LC}}\ (\text{in Hz})\,, \tag{2}$$

$$\textit{Damping Ratio} = \frac{1}{2R}\sqrt{\frac{L}{C}}\,. \tag{3}$$

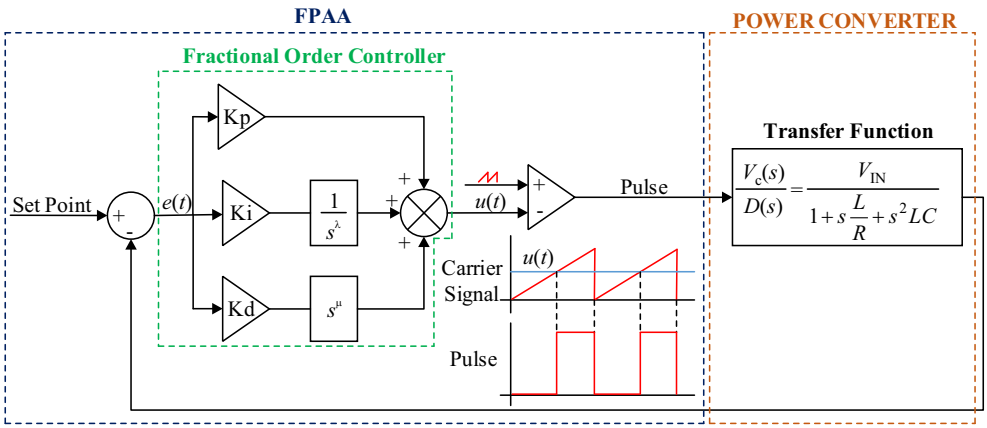

Fig. 2. Simulink closed loop control scheme with a synchronous buck converter model

Table 1. : Converter specification

Input Voltage	12 V
Regulated Output voltage	3 V
Switching frequency	10 kHz
Inductor current ripple	30%
Output voltage ripple	10 mV

Table 2. Converter parameters

Inductor L	750 μH
Capacitor C	375 μF
R_{LOAD} nominal	3 Ω
Duty Ratio D	0.25

Table 3. Controller parameters

Type	K_p	K_i	K_d	λ	μ
IOPID	0.97	349.84	0.00022	—	—
FOPID	24.01	0.52	0.002	0.001	1.04
IOPI	0.01	30	—	—	—
FOPI	0.001	60	—	1.1	—

Table 4. Transient performance

Type	Settling time	Rise time	Under-shoot
IOPID	456.85 s	368.17 s	—
FOPID	314.84 s	318.69 s	—
IOPI	9.48 ms	4.73 ms	3.51%
FOPI	6.20 ms	1.38 ms	0.01 %

2.1 Inductor selection

In switching power supply, the inductors function is to maintain a constant current or sometimes to limit the rate of change of current flow. The inductor value and its peak value are determined based on the specific maximum value of its peak current ripple as

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} F_{SW} \Delta I_L}. \tag{4}$$

The peak inductor current ripple is selected within the range of 30–40 % [8] whereas FSW is the switching frequency.

2.2 Capacitor selection

The role of capacitor inside the DC buck converter is to prevent voltage from dropping to zero and to store energy or charges when the switches are closed. Furthermore, it filters the ripple current of inductor and ensures that the voltage overshoot is minimized. The capacitor value can be calculated from

$$C = \frac{\Delta I_L}{8 \times F_{SW} \times \Delta V_{OUT}} \tag{5}$$

where ΔV_{OUT} is the output voltage ripple.

2.3 Selecting power switch

The power switch MOSFET would be selected based on its characteristics and behavior. It has the advantages of higher communication speed and high efficiency when operating at low voltage. It can also tolerate high blocking voltage and sustain high current. However, MOSFET comes in two types, namely n-channel and p-channel MOSFET. The p-channel MOSFET is widely accepted in a buck power stage since the driving of gate is simpler when compared to n-channel type.

3 Control technique and tuning parameters

The nominal values of the synchronous buck converter are given in Tab. 1 and Tab. 2 and its parameters are calculated. Accordingly, one can first implement the DC/DC buck converter in the MATLAB Simulink together with one controller type. Before hardware verification, the controller parameters were calculated for integer PI/PID and

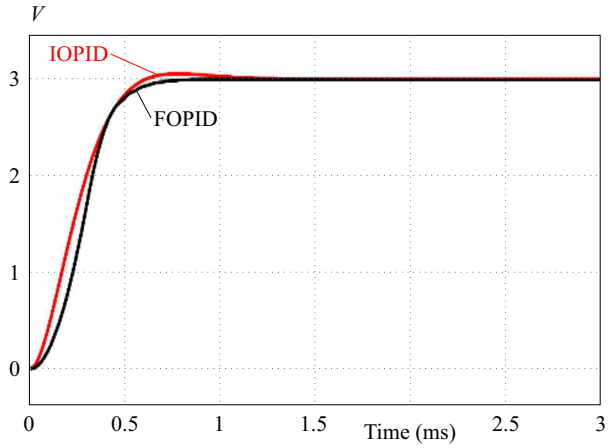

Fig. 3. IOPID and FOPID controller response

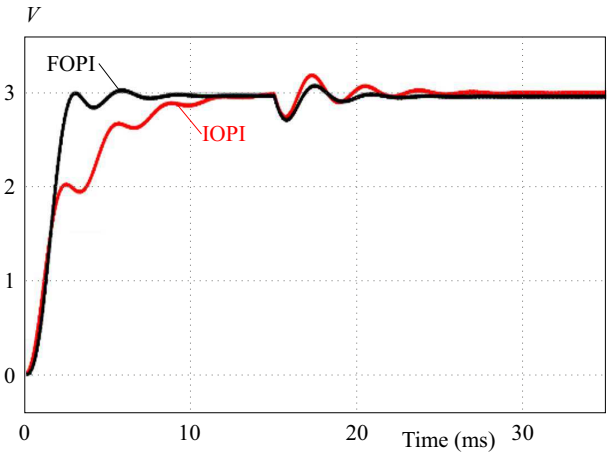

Fig. 5. FOPI vs IOPI with load disturbance

Table 5. : Measure voltage outputs

Buck Converter	Regulated Output Voltage	Inductor Current
Conventional	2.376 V	0.6342 A
Synchronous	2.971 V	0.8423 A

fractional PI/PID. Using (1), the following buck converters mathematical model is obtained

$$\frac{V_c(s)}{D(s)} = \frac{12}{(2.8125 \times 10^{-7})s^2 + 0.00025s + 1} \tag{6}$$

The closed loop configuration of the proposed output regulation scheme for the synchronous buck converter is shown in Fig. 2. It is considered that the most commonly used structures of IOPID and FOPID respectively are

$$C_{PID}(s) = \mathrm{K_p} + \mathrm{K_i}(s^{-1}) + \mathrm{K_d}(s), \tag{7}$$

$$C_{FPID}(s) = \mathrm{K_p} + \mathrm{K_i}/s^{\lambda} + \mathrm{K_d}s^{\mu} \tag{8}$$

where $\mathrm{K_p}$, $\mathrm{K_i}$ and $\mathrm{K_d}$ are proportional, integral and derivative gains and (λ, μ) are any positive real number.

Based on this model, both integer PID and the fractional PID parameter were tuned using Whale optimization algorithm [12] for integer and FOMCON toolbox [13]

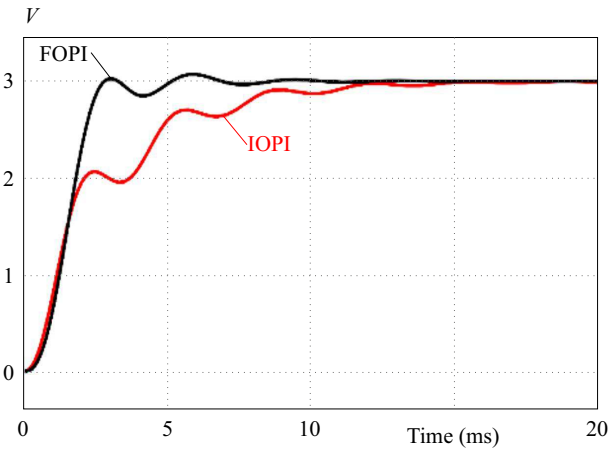

Fig. 4. IOPI and FOPI controller responses

for fractional controllers. Note that both controller parameters are calculated with the same performance index known as ITAE minimization. The tuned parameters are listed in Tab. 3.

From the results obtained in simulation, it is clear that FOPI(D) outperforms the IOPI(D) with respect to performance measures as shown in Tab. 4. Nevertheless, FOPID control can be more difficult to tune due to more parameters in the tuning process. Other the other hand, it will offer more freedom for robust control due to fractional derivative or integral. The performance of the buck can be degraded in presence of large load disturbances as the output voltage is difficult to regulate through PWM. The performance of the controller has been tested with the input additional load disturbance of 0.25 A. The load is added to the system at time 0.015 s. The test with load disturbance and comparison with PI, in Fig. 5 depicts clearly that FOPI takes less time to settle down.

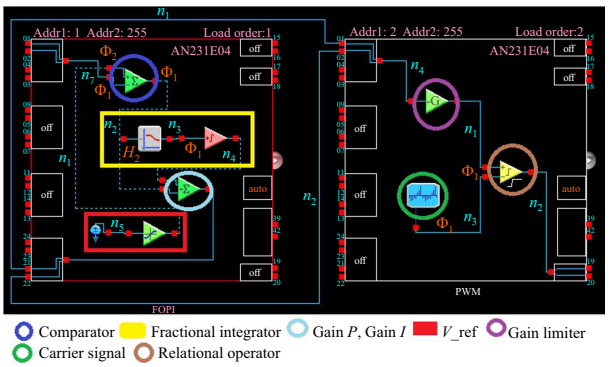

Fig. 6. Overall system configuration and setup

In order to check the performance between the conventional and synchronous buck converters, the closed loop control for both converter models were developed. As noted in [12], the synchronous converter can improve the efficiency up to 5 % in whatever result one can obtain from conventional buck converter. Table 5 shows the measured outputs from the both type of converters from the designed model and controller values. Again, the claim is agreed upon.

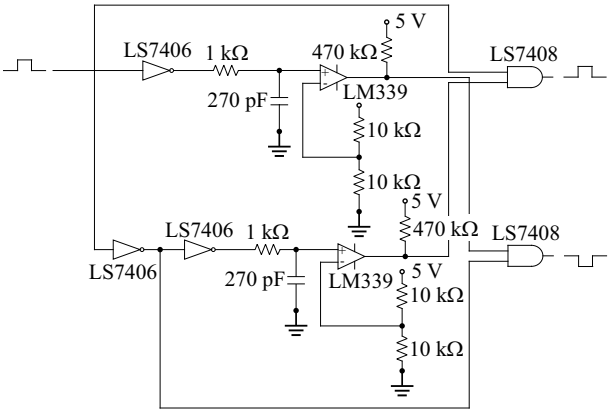

Fig. 7. Controller in FPAA board

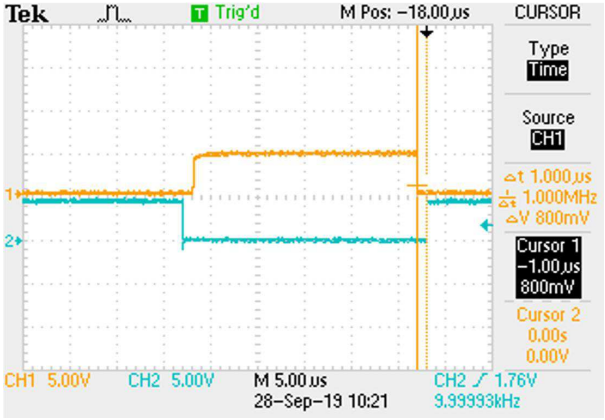

Fig. 8. Dead time circuit

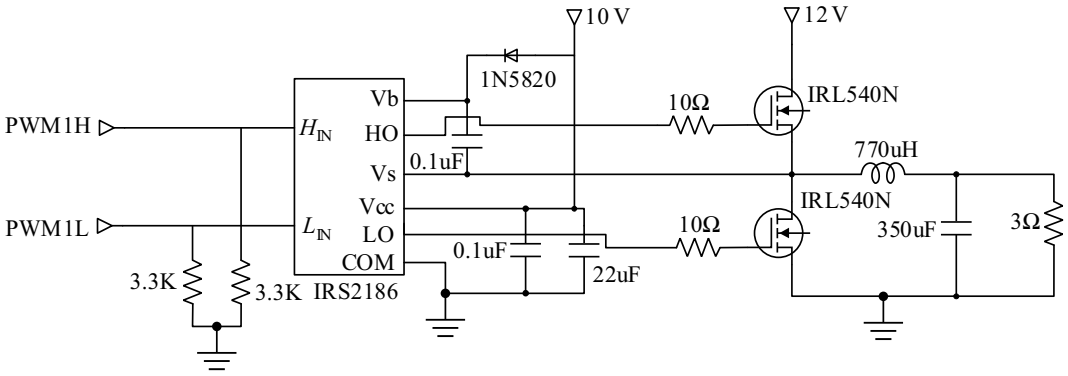

Fig. 9. Dead time incorporated in the compliment pulses

Fig. 10. The controlled output from the DC-DC buck converter using FOPI

4 Real-time controller realization with FPAA

The FPAA is an integrated circuit device that has reconfigurable feature with computing continuous signal. This reprogrammable device can operate in both continuous and discrete time. To note that there was a history about FPAA, where it had a few programmable element with limited interconnection capabilities and resolution issue. Now, the application on hand is more beneficial, especially when comparing with FPGA. Unlike FPGA, the application of FPAA tends to be more driven than general purpose as they may be current mode or voltage mode devices. In particular to this research, a successful analog PI controller for DC servo position was tested on FPAA circuit in a loop [14]. In general, FPAA has a block to setup an operational amplifier in combination with programmable configuration of passive components. Recently, the analog fractional integrator and derivative were presented [7] for FOPI, to show the efficacy of fractional controller for real-world application.

Let us now understand the overall application of DC-DC buck converter together with feedback in a loop. Aiming to sense the voltage from a voltage divider which goes into single to differential circuit before going into the FPAA. This is referred to as feedback signal. A block diagram representation for DC-DC buck converters voltage control is presented in Fig. 6. The output from the FPAA is a pulse of $5V_{p\text{-}p}$ which is reconverted back to single ended signal by the aid of differential to single converter before going to the driver circuit where the later steps the pulse to a require gate voltage of the power converter.

Figure 7 shows the implementation of the fractional order PI controller in FPAA using Anadigm Designer 2 software. The FOPI controller requires only one address block (AN231E04) and the implementation of the PWM is realized in the second address.

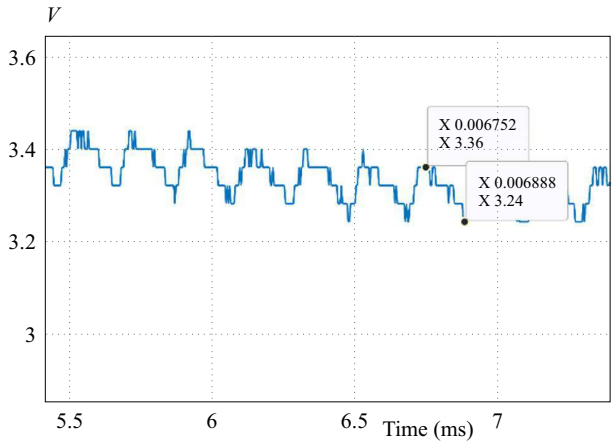

Fig. 11. The output ripple voltage

The dead time circuit was constructed (Fig. 8) in order to split the output PWM from the controller with a dead time delay. This is crucial as in synchronous mode of operation of the power converter, both switches should not be active at the same time or else the input source can be short-circuited. The pulse difference is kept to 1 μs using delay logic circuit as displayed in Fig. 9.

The PWM output from the dead time circuit is step from $5V_{p\text{-}p}$ to $10V_{p\text{-}p}$ by the driver circuit to meet the required gate-source voltage (V_{GS}) of the two MOSFETs. This is achieved with the power MOSFET driver IRS2186. The circuit diagram is shown in Fig. 10.

The results agree with the theoretical calculated values for the rise time and settling time as per Tab. 4. An overshoot can be seen and this may be due to the multiple switch that has to be turn on and off at the same time. However, a small undershoot is also observed as per simulation study. The voltage ripples correlate with the theoretical assumption (refer to Tab. 1), which is 10 mV, where the experimental value came as 12 mV (shown below in Fig. 12). It is to be noted that this scheme is not only simple to implement but also exact system parameters are not required. Finally, the validity and usefulness of the control scheme is verified by simulation as well as hardware agreements with the objective of the work.

5 Conclusins

The paper concentrates on a controller where output voltage of synchronous DC buck converter was designed to be monitored by FPAA. The system was studied and modelled on MATLAB/Simulink before it was implemented on hardware. The FPAA was used to design the FOPI controller and pulse. The suitable FOPI parameters were tuned to verify the performance with respect PID. The solution is provided to interface FPAA with measurement circuits and the DC synchronous buck converter. The dead time circuit was designed to create a delay time between the switching MOSFET inside the DC buck converter. It is seen the practical circuit performs well with proposed modulation method. The comparative study conquers how such fractional-order adoption performs better than conventional PID. It has been noted with better dynamic performance especially to the uncertain load and operating gap. The future work of this study is to monitor the current as well as voltage using FPAA. Since both current and voltage are inversely proportional due to load connected to the controller, it will identify the exact limitation of the load. The efficacy of the analog controller has demonstrated in this paper and has given some directions to adopt the new fractional analog controller.

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