ELEMENTARY-TREE SPACE COMPRESSION USING COMBINATION OF NONLINEAR AND LINEAR LOGIC

Sunil R. Das[1, 2], Nick Malan[1], Scott Morton[1], Satyendra N. Biswas[3], and Mansour H. Assaf[4]

[1]Department of Computer Science, College of Arts and Sciences
Troy University, Montgomery, AL 36103, USA
[2]School of Information Technology and Engineering, Faculty of Engineering
University of Ottawa, Ottawa, ON K1N 6N5, Canada
[3]School of Engineering and Computer Science
Kaziranga University, Jorhat 785006, Assam, India
[4]Department of Electrical and Electronic Engineering
University of the South Pacific, Suva 19128, Fiji

Introduction

With tremendous growth in the field of microelectronics, the integration densities and system complexities increased considerably and hence, the need for better and more effective methods of testing to assure reliable operation of integrated circuit (IC) chips, the mainstay of today's many sophisticated devices and products, was intensely felt [1]–[5]. The conventional testing procedures of digital systems require application of test vectors generated by a test pattern generator (TPG) to the circuit under test (CUT) and comparison of the produced responses with the correct ones. For very large scale integrated (VLSI) systems, because of higher storage requirements for the fault-free responses, the standard test processes become highly expensive and thus, alternative approaches are sought at minimizing the amount of required storage. Built-in self-testing (BIST) is a design philosophy that has the capability of solving many of the problems otherwise encountered in testing digital systems. It combines the concepts of built-in test (BIT) and self-test (ST) in *one*, termed BIST. In BIST, test generation, test application and response verification are all accomplished through built-in hardware. This allows different parts of an IC chip to be tested in parallel, thereby reducing the testing time besides eliminating the need for external test equipment. A typical BIST architecture uses a TPG that sends its outputs to a CUT and output bit streams from the CUT are fed into a test data analyzer. A fault is detected if the test sequence is different from the response of the fault-free circuit. The test data analyzer is comprised of a response compaction unit (RCU), storage for the fault-free response of the CUT and comparator.

In an effort to reduce the amount of data represented by the fault-free and faulty CUT responses, data compression is used to create signatures (short binary sequences) from the CUT and its corresponding fault-free circuit. BIST techniques use pseudo-exhaustive or exhaustive test patterns or on-chip storing of reduced or compact test sets. The RCU can be split into two parts: a space compaction unit followed by a time compressor. In general, $\mathbf{P}$ input sequences coming from a CUT are fed into a space compressor, providing $\mathbf{L}$ output streams of bits such that $\mathbf{L} \ll \mathbf{P}$; most often, test responses are compressed into only one sequence ($\mathbf{L} = 1$). Space compression provides a viable solution to the problem of achieving high quality BIST of complex circuit chips without the necessity of monitoring a large number of internal test points to reduce testing time and area overhead through merger of test sequences coming from the internal test points to a single stream of bits. This single bit stream of length $\mathbf{H}$ is eventually fed to a time compactor, generating a shorter sequence of length $\mathbf{B}$ ($\mathbf{B} < \mathbf{H}$) at the output.

In the subject paper, our focus is on the problem of response data compaction of multi-output digital circuits with a view to designing aliasing-free space compression networks for BIST using pseudo-random and compact test sets. With this perspective in target, the paper proposes technique for implementing aliasing-free BIST space support hardware, extending some well-known concept of conventional switching theory, *viz.* that of compatibility relation as employed in the minimization of incomplete sequential machines, based on pairwise sequence mergeability, for detectable single stuck-line faults of the CUT. Using mathematically sound selection criteria of aliasing-free merger of a pair of response data outputs of the CUT by two-input AND/NAND and/or XOR/XNOR logic, the paper achieves maximal compaction in the design, as is evident from the simulation runs conducted on the International Symposium on Circuits and Systems (ISCAS) 85 combinational and ISCAS 89 full-scan sequential benchmark circuits using fault simulation programs ATALANTA [6], FSIM [7] and HOPE [8]. Only some limited results on simulation on ISCAS 85 and ISCAS 89 full-scan sequential benchmark circuits using the simulation programs are provided here though.

The mathematical basis underlying the realization of the proposed aliasing-free space compression is not discussed here as well. Fundamentally, based on the notion of AND/NAND and/or XOR/XNOR fault detection (FD) compatibility and *conditional* FD compatibility, optimal pairs of lines can be selected at the output of the original CUT and at subsequent stages of the compaction process. The process of merger has to be continued until all output lines or as many as possible are exhausted at each compression stage, eventually obtaining an aliasing-free compactor, preferably with a single output line. The algorithm details for the selection of a maximal number of two-input AND/NAND and/or XOR/XNOR logic at each stage of compaction based on the concept of FD compatibility and *conditional* FD compatibility [5] could not also be furnished because of space constraint.

Simulation Experiments

To demonstrate the feasibility of the proposed aliasing-free space compression technique, independent simulations were conducted on ISCAS 85 combinational and ISCAS 89 full-scan sequential benchmark circuits. In the design experimentation, we used ATALANTA [6] (fault simulation program developed at the Virginia Polytechnic Institute and State University) as our test generation tool to provide the fault-free output sequences required to construct the space compressor circuits and to test the benchmark circuits using reduced test sets, accompanied with random test sessions with FSIM and HOPE fault simulation programs [7], [8] that produce the necessary pseudo-random test vectors that detect most detectable single stuck-line faults for all the benchmark circuits. For each of the circuits, we computed the fault coverage (FC) before adding the compaction network, FC with the compression circuit, number of applied test vectors, simulation CPU time, estimates of hardware overhead and maximal compaction ratio. In Figures 1 and 2 are given only limited simulation results on ISCAS 85 and ISCAS 89 full-scan sequential benchmark circuits using ATALANTA, FSIM and HOPE.

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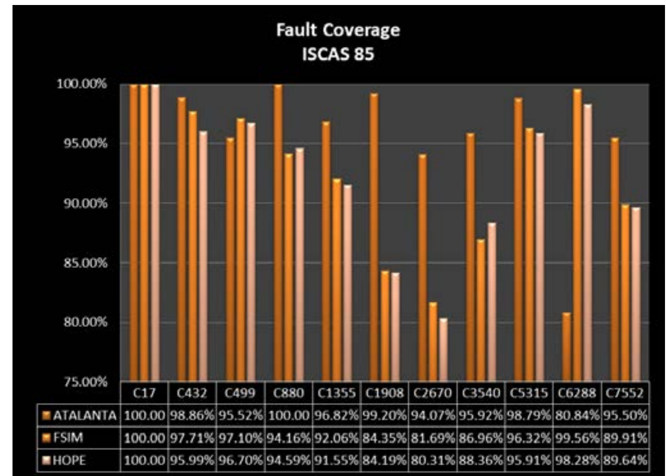

	C17	C432	C499	C880	C1355	C1908	C2670	C3540	C5315	C6288	C7552
ATALANTA	100.00	98.86%	95.52%	100.00	96.82%	99.20%	94.07%	95.92%	98.79%	80.84%	95.50%
FSIM	100.00	97.71%	97.10%	94.16%	92.06%	84.35%	81.69%	86.96%	96.32%	99.56%	89.91%
HOPE	100.00	95.99%	96.70%	94.59%	91.55%	84.19%	80.31%	88.36%	95.91%	98.28%	89.64%

Figure 1.Fault coverage for ISCAS 85 combinational benchmark circuits using ATALANTA, FSIM and HOPE.

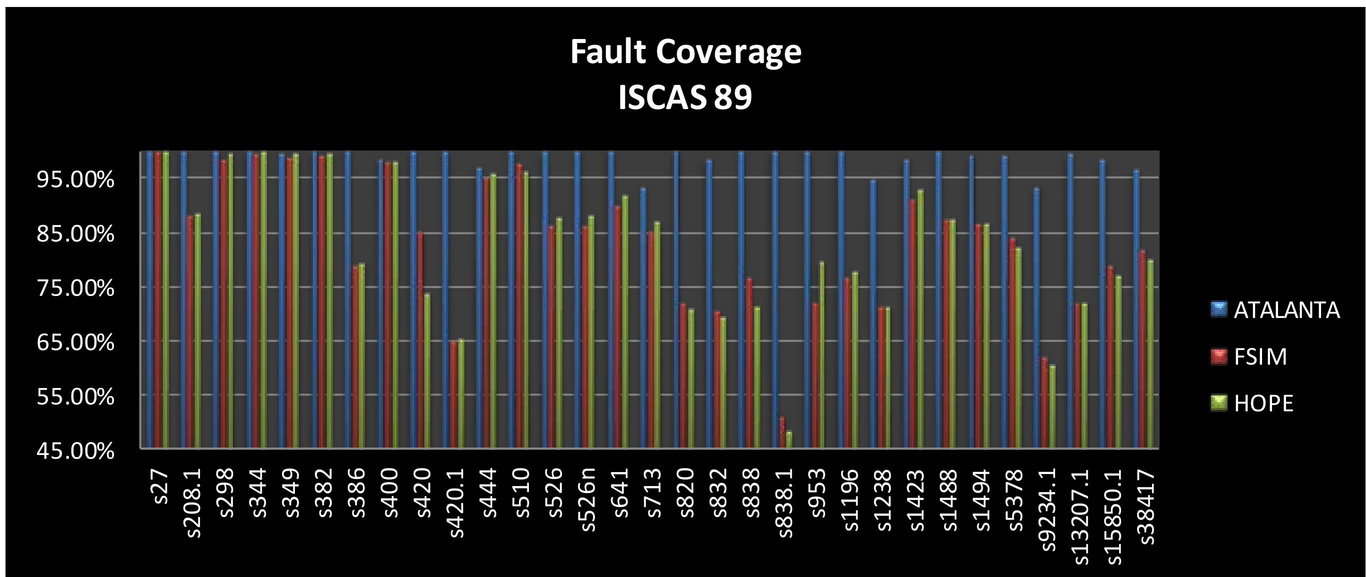

Figure 2. Fault coverage for ISCAS 89 full-scan sequential benchmark circuits using ATALANTA, FSIM and HOPE.